REMARKS

Pending Claims

Claims 1-12 are pending. Claims 1, 2 and 5 have been amended to correct informalities without affecting the scope of the claims. No new matter has been added.

Specification

A new Abstract of the Disclosure has been supplied in accordance with the Examiner's requirement.

Claim Rejections Under 35 U.S.C. §102

Claims 1-12 are rejected under 35 U.S.C. §102(e) as being anticipated by Vu et al, U.S. Patent No. 6,654,066. Applicants request reconsideration of the rejection for the following reasons.

The present invention is directed to a D/A converter circuit having first and second current mirror circuits. The first current mirror circuit includes input side transistors TNa and TNp, the drains of which are connected to an input terminal 11a of the D/A converter circuit 11, as shown in Fig. 1. The output side transistors TNb to TNi of the current mirror circuit correspond to digits of 8-bit display data, respectively. See digits D0 – D7, as shown in Figure 1. The display data D0 to D2 correspond to 3 digits having weights less than 1, that is, 1/8, 1/4, 1/2. The drains of the output side transistors TNb to TNd corresponding to digits D0

to D2 are connected to (second) current mirror circuits 111, 112 and 113 provided on the upstream side, respectively. The output side transistors of the current mirror circuits 111, 112 and 113 are connected to an output terminal 11b of the D/A converter circuit 11 through an output line 114, respectively.

For example, as shown in Figure 1, a (second) current mirror circuit is formed by input transistor QN1 and output transistor QN2 having output side transistors TN1 and TN2. The operating current ratio of the output side transistor of the second current mirror circuit with respect to an input side transistor of the second current mirror circuit is set to n : 1. See page 13, line 25 to page 14, line 17 of the specification. The analog current is generated by obtaining a current corresponding to the weight of the digit on the output side transistor (TN2) of the (second) current mirror circuit 111.

The claimed embodiment of the invention is directed to a D/A converter circuit having a first current mirror circuit corresponding to digits of data to be converted and a second current mirror circuit connected on an upstream or downstream side of at least one of the output side transistors corresponding to a lower digit of the data being converted. The second current mirror circuit is further claimed as having an operating current ratio of an output side transistor of the second current mirror circuit with respect to an input side transistor of the second current mirror circuit that is set to n : 1. On the other hand, Vu discloses an interface circuit having a DAC 210, DAC 220 and an ADC 250. As shown in Figure 2, the interface circuit includes first and second current mirror circuits, however these

current mirror circuits are not comparable to the first and second current mirror circuits claimed by applicants in claim 1.

In Vu, the first current mirror circuit provides for a full-scale offset current (I_{OSFS}) to the DAC 220 and the second current mirror circuit that outputs a current that is related to the gain scaled current (IGAIN). Additionally, a third current mirror circuit provides an offset current (IOS) for the DAC 220, and a fourth current mirror circuit provides a fourth current related to the offset current IOS for the DAC 220. The current mirror circuits disclosed by Vu do not correspond to digits of data to be converted for generating an analog current, as in the present invention. Further, Vu does not disclose first and second current mirror circuits in which the second current mirror circuit is connected on an upstream or downstream side of at least one of the output side transistors corresponding to a lower digit of the data, wherein an operating current ratio of the output side transistor of the second current mirror circuit with respect to an input side transistor thereof is set to n : 1 (where n is a positive integer) and the analog current is generated by obtaining a current corresponding to a weight of the lower digit, which is less than 1, on the output side transistor of the second current mirror circuit. Accordingly, Vu does not anticipate the invention set forth in claims 1-12 by applicants. Therefore, the rejection under 35 U.S.C. §102(e) should be withdrawn.

Conclusion

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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